**Independent Claim 2, and Dependent Claims 6-10**

Amended independent claim 2 recites, among other features, a semiconductor memory device that includes a plurality of transistors formed two by two in each of a plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of the source/drain diffusion layers is positioned over trenches of two adjacent trench capacitors, the transistors each having a gate connected to a word line continuous in one direction; and a contact layer for connecting the other of the source/drain diffusion layers of each of the transistors to a capacitor node layer of corresponding one of the trench capacitors. Some embodiments of the novel claim 2 device permit a greater reduction in cell size as compared to the systems of the prior art, allowing for a higher concentration of elements in the device.

The Action rejected independent claim 2, and dependent claims 6-10, under 35 U.S.C. 102(b) as being anticipated by *Park et al.* In rejecting claim 2, the Action alleges that *Park et al.* shows the following features: semiconductor substrate 10, trench capacitor node layers 55, semiconductor layers 32/58, element isolation insulating film 30, transistors 14 sharing source/drain 18, and other source/drain 20 positioned over region 32, transistor gate 16/62 connected to continuous word line, and contact layer 26 connecting source/drain layer to node layers and bit line contacts 78. Action, p. 3. The Action also states that N-region 32, insulating collar 28, and region 55 together form a trench capacitor, and that region 20 is located over "the capacitor's region" because the region 20 is over N-region 32. Action, p. 5.

Using the Action's application of the *Park et al.* patent to the claims, it is clear that the *Park et al.* patent does not teach or suggest the novel invention recited in amended claim 2. For example, *Park et al.* fails to teach or suggest region 20 (the alleged other of the source/drain

diffusion layers) being positioned over trenches of two adjacent trench capacitors, as recited in amended claim 2. Indeed, the *Park et al.* region is expressly stated to be adjacent to the trench in which the region 55 is formed. *Park et al.*, col. 5, lines 8-10. See also *Park et al.* Fig. 10.

None of the additional references cited in the Action (*Ishii*, *Bronner et al.* and *Ushiku et al.*) overcomes the deficiencies identified above with respect to *Park et al.* For at least these reasons, Applicants respectfully submit that amended claim 2 distinguishes over the cited references, and is in condition for allowance.

The Action relies on the same analysis of *Park et al.* to reject dependent claims 6-10 as being anticipated. However, claims 6-10 recite various additional features that are absent from *Park et al.* For example, claim 6 recites "[t]he semiconductor memory device according to claim 2, wherein said contact layer is buried such that said contact layer extends through the other of said source/drain diffusion layers to reach said capacitor node layer." In applying *Park et al.* to this claim, the Action alleges that the *Park et al.* conductive strap 26 shows the claimed contact layer, that the *Park et al.* region 20 shows the claimed other of said source/drain diffusion layers, and that the *Park et al.* layer 55 shows the claimed capacitor node layer. Action, p. 3. Contrary to the Action's allegations, however, *Park et al.* Fig. 10 demonstrates that conductive strap 26 is not "buried such that said contact layer extends through the other of said source/drain diffusion layers to reach said capacitor node layer," as recited in dependent claim 6.

As another example, claim 7 depends from claim 2, and recites, among other features, that "the other of said source/drain diffusion layers has a bottom surface connected to a top surface of said contact layer." As shown in *Park et al.* Fig. 10, storage node 20 (the alleged other of the source/drain diffusion layers) does not have a bottom surface connected to a top surface of

conductive strap 26 (the alleged contact layer). Dependent claim 10 also recites this claim feature (among others). Accordingly, dependent claims 6-10 are distinguishable from the cited art for at least the reasons discussed above, and those set forth above with respect to claim 2.

**Dependent Claims 3-5**

The Action rejected dependent claims 3-5 under 35 U.S.C. 103 as being obvious over *Park et al.* in view of *Ishii*. In doing so, the Action concedes that *Park et al.* does not teach the shape, dimension and arrangement recited in these dependent claims. Action, p. 4. The Action cites *Ishii* to show various trench 8 arrangements (see *Ishii* Figs. 5 and 7), but cites nothing to show the recited dimensions of the capacitors in claims 3 and 4. Instead, the Action simply states that it would have been obvious to use the minimum processing dimensions. Action, p. 5. Even assuming the Action were correct in this regard, the Action still fails to explain its contention that it would have been obvious to have the capacitors "shaped substantially in a square having one side equal to 2F, where F is a minimum processing dimension," as recited in each of claims 3 and 4. Furthermore, the Action does not mention anything at all regarding the pitch arrangements recited in claims 3-5, and cites to no specific teaching or suggestion to combine these references as suggested in the Action. Applicants respectfully submit that dependent claims 3-5 are distinguishable over *Park et al.* in view of *Ishii*, even if the references were properly combinable. Accordingly, dependent claims 3-5 are distinguishable from the cited art for at least the reasons discussed above, and those set forth above with respect to claim 2.

**Dependent Claim 11**

The Action rejected dependent claim 11 under 35 U.S.C. 103 as being obvious over *Park et al.* in view of *Bronner et al.* In making this rejection, the Action relies on *Park et al.* for the

features recited in claims 2 and 10, and *Bronner et al.* to show the features added by claim 11. The Action generally alleges that *Bronner et al.* teaches "two layer isolation films." but does not cite to any specific teaching within the *Bronner et al.* reference for such films, or for the specific features recited in claim 11. Action, p. 4. The Action does refer to "Paragraph 12," but paragraph 12 of the Action merely lists the field of the Examiner's search for the Action. Applicants believe the Action's reference to "Paragraph 12" may have been intended to reference Paragraph 12 of the previous Action, which discussed *Bronner et al.,* but as applied to claim 12. However, and as discussed in the previous Amendment and Response, Paragraph 12 of the previous Action cites to the *Bronner et al.* P+ layer 18 and Silicon layer 14, which are not insulating films. Even assuming that the Action is correct, and *Bronner et al.* does teach "two-layer isolation films," such a teaching would still fail to teach or suggest the particular features recited in claim 11. For example, claim 11 recites, among other features, "a substrate isolation insulating film is interposed on a bonding surface of said semiconductor substrate and said other semiconductor substrate bonded thereto." The Action does not point to any teaching or suggestion in *Bronner et al.* for such a feature.

Furthermore, claim 11 recites the additional feature of "said element isolation film includes a first element isolation insulating film buried in element isolation regions in the bit line direction to a depth at which said first element isolation insulating film reaches said substrate isolation insulating film; and a second element isolation insulating film partially overlapping said first element isolation insulating film and buried in element isolation regions in the bit line direction and word line direction to a depth shallower than said first element isolation insulating film." *Bronner et al.* lacks any teaching or suggestion, and the Action cites none, for such a first element isolation insulating film, second element isolation insulating film, and the recited

relationships between the two. Accordingly, Applicants submit that dependent claim 11 is distinguishable from the cited art for at least the reasons discussed above, as well as those set forth above with respect to claims 2 and 10, from which claim 11 depends.

**Independent Claim 12, and Dependent Claim 18**

The Action alleges that independent claim 12, and dependent claim 18, are each anticipated by *Ushiku et al.* In particular, the Action cites *Ushiku et al.* Fig. 10, focusing on the argument that substrate 81, oxide layer 85 and oxide layer 94 are shallower and wider than oxide 85. Regarding dependent claim 18, the Action cites diffusion region 93 to show the claimed contact layer, stating that diffusion region 93 is formed underneath oxide 94 and beside oxide 85. Action, p. 2.

Amended independent claim 12 recites, among other features, "an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film shallower and wider than said first insulating film and positioned over the first insulating film;" and "elements formed in said active element areas defined by said element isolation insulating film, said elements including a capacitor node formed in a trench in said semiconductor substrate, and a contact layer contacting an upper surface of said capacitor node, wherein said contact layer is formed in a contact hole in said semiconductor substrate." Some embodiments of the claim 12 device permit greater accuracy during the manufacturing process.

*Ushiku et al.* fails to teach or suggest the claim 12 device. For example, *Ushiku et al.* neither teaches nor suggests a capacitor node formed in a trench in said semiconductor substrate, and diffusion region 93 (alleged to be the claimed contact layer) "contacting an upper surface of

said capacitor node, wherein said contact layer is formed in a contact hole in said semiconductor substrate," as recited, among other features, in Applicants' amended independent claim 12.

Applicants respectfully submit that amended independent claim 12 distinguishes over the cited art, and is in condition for allowance.

Claim 18 depends from independent claim 12, and is allowable for at least the same reasons as claim 12, and further in view of the various advantageous and novel features recited therein. For example, amended dependent claim 18 recites "[t]he device of claim 12, wherein said contact layer contacts an underside of second insulating film, and a side of the first insulating film." As noted above, the Action has cited the *Ushiku et al.* diffusion region 93 to show the claim 12 contact layer, oxide layer 85 to show the claimed first insulating film, and layer 94 to show the claimed second insulating film. As is shown in *Ushiku et al.* Fig. 10, this reference simply fails to teach or suggest these recited features.

**Conclusion**

For at least the foregoing reasons, Applicants respectfully submit that claims 2-12 and 18 are distinguishable from the cited art, and are in condition for allowance. If the Examiner feels that further discussion and/or amendment may be helpful in placing this application in condition for allowance, the Examiner is invited to telephone the Applicants' undersigned representatives at the number appearing below.

[SIGNATURE PAGE FOLLOWS]

Respectfully submitted,

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## MARKED-UP VERSION OF AMENDED CLAIMS

Applicants respectfully request that claims 2, 12 and 18 be amended as follows:

2. (Amended) A semiconductor memory device comprising:

a semiconductor substrate;

a plurality of trench capacitors formed in said semiconductor substrate and arranged at a regular pitch;

a semiconductor layer formed on said semiconductor substrate in which said trench capacitors are formed;

an element isolation insulating film buried in said semiconductor layer to define a plurality of active element areas each spreading over two adjacent trench capacitors;

a plurality of transistors formed two by two in each of said plurality of active element areas, such that two transistors share one of source/drain diffusion layers, and the other of said source/drain diffusion layers is positioned over ~~regions~~ trenches of two adjacent trench capacitors, said transistors each having a gate connected to a word line continuous in one direction;

a contact layer for connecting the other of said source/drain diffusion layers of each of said transistors to a capacitor node layer of corresponding one of said trench capacitors; and

a bit line provided to intersect said word lines and connected to one of said source/drain diffusion layers of said transistor.

12. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate;

an element isolation insulating film including a first insulating film buried to define active element areas on said semiconductor substrate, and a second insulating film

shallower and wider than said first insulating film and positioned over the first insulating film; and

elements formed in said active element areas defined by said element isolation insulating film, said elements including a capacitor node formed in a trench in said semiconductor substrate, and a contact layer contacting an upper surface of said capacitor node, wherein said contact layer is formed in a contact hole in said semiconductor substrate.

18. (Amended) The device of claim 12, ~~further comprising a~~wherein said contact layer contacts an underside of ~~formed underneath the~~ second insulating film, and ~~beside~~ a side of the first insulating film.